Model Curriculum

NOS Name: Foundation of System on Chip (SoC) Design
OEM Name: System on Chip (ARM Cortex-M0) Design Foundation

NOS Code: ELE/MCr-0002

NOS Version: 1.0

NSQF Level: 4

Model Curriculum Version: 1.0

Electronics Sector Skills Council of India || 155, 2nd Floor ESC House, Okhla Industrial Area – Phase 3, New Delhi - 110020

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Training Parameters

Sector	Electronics
Sub-Sector	Semiconductor & Components
Occupation	Product Design-S&C
Country	India
NSQF Level	4
Aligned to NCO/ISCO/ISIC Code	NCO-2015/2512.0501
Minimum Educational Qualification and Experience	1. 2nd year of 3 year diploma after 10th No experience required 2. 12th or Equivalent No experience required 3. 10 3 years of relevant experience 4. Previous NSQF qualifications of Level 3 with 3 years of relevant experience
Pre-Requisite License or Training	NA
Minimum Job Entry Age	18
Last Reviewed On	27.08.2024
Next Review Date	27.08.2027
NSQC Approval Date	27.08.2024
NOS Version	1.0
Model Curriculum Creation Date	27.08.2024
Model Curriculum Valid Up to Date	27.08.2027
Model Curriculum Version	1.0
Maximum Duration of the Course	30 Hrs.

Program Overview

This section summarizes the end objectives of the program along with its duration.

Training Outcomes:
At the end of the program, the learner should have acquired the listed knowledge and skills:

Compulsory:

- Basic lecture introduces different aspects of Electronics and exposure to the current activities at a particular.

Compulsory Modules:
The table lists the modules and their duration corresponding to the Compulsory NOS of the QF.

NOS and Module Details	Theory / Demonstration Duration (In Hours)	Practical/OJT Duration (In Hours)	On-the-Job Training Duration (in hours) (Mandatory)	On-the-Job Training Duration (in hours) (Recommended)	Total Duration (In Hours)
ELE/MCr-0002	15:00	15:00	00:00	00:00	30:00
Module 1: Introduction to SoC Design and Architecture	15:00	15:00	00:00	00:00	30:00
Total Duration	**15:00**	**15:00**	**00:00**	**00:00**	**30:00**

Module Details

Module 1: Introduction to SoC Design and Architecture

Mapped to ELE/MCr-0002

Terminal Outcomes:

Upon completion of the module on Introduction to SoC Design and Architecture, students will be able to:

- Understand and explain the significance and components of System-On-Chip (SoC) design.
- Set up and configure ARM Cortex-M0 development environments for embedded systems.
- Develop and test basic to intermediate ARM assembly and C programs, integrating peripherals and handling interrupts.

Duration: 15:00 hrs
Theory - Key Learning Outcomes
• Explain the significance of SoC development and the integration of multiple functions onto a single chip. • Define SoC and describe its key components, including core registers and memory maps. • Outline the ARM Cortex-M0 processor architecture, including its core components like the Nested Vectored Interrupt Controller (NVIC) and Debug System. • Discuss the principles and elements of the AMBA 3 AHB-Lite bus architecture and their roles in data transfer. • Highlight the advantages and limitations of C and assembly programming languages in embedded systems. • Introduce the Cortex Microcontroller Software Interface Standard (CMSIS) and its components for software development.
Duration: 15:00 hrs
Practical - Key Learning Outcomes
• Set up and configure an ARM Cortex-M0 development environment, including relevant software tools and hardware platforms. • Write and test simple ARM assembly code, focusing on basic instructions and program flow. • Implement a basic SoC configuration with the Cortex-M0 processor and AHB-Lite bus, integrating peripherals like LEDs and switches. • Configure and manage advanced peripherals such as timers and GPIOs for versatile I/O functionalities.

• Develop CMSIS-based device drivers and APIs, and create applications like a single-player snake game using C and assembly.
Classroom Aids: (If Offline mode)
• Whiteboard and Markers • Chart paper and sketch pens • LCD Projector and Laptop for presentations
Tools, Equipment and Other Requirements
Labs equipped with the following: • ARM Cortex-M0 development boards, such as STM32 Nucleo or similar. • Software tools: Keil MDK, CMSIS, ARM GCC.

Annexure

Trainer Requirements

Trainer Prerequisites						
Minimum Educational Qualification	**Specialization**	**Relevant Industry Experience**		**Training Experience**		**Remarks**
		Years	**Specialization**	**Years**	**Specialization**	
Graduate Science & Engineering	Electrical/ Mechanical/ Electronics	1	Semiconductor Technology, Embedded System	1	Semiconductor Technology, Embedded System	
Diploma/ITI	Electrical/ Mechanical/ Electronics	2	Semiconductor Technology, Embedded System	1	Semiconductor Technology, Embedded System	

Trainer Certification	
Domain Certification	**Platform Certification**
"**Foundation of System on Chip (SoC) Design**, ELE/MCr-0002, version 1.0". Minimum accepted score is 80%.	Recommended that the Trainer is certified for the **Foundation of System on Chip (SoC) Design** "Trainer (VET and Skills)", mapped to the Qualification Pack: "MEP/Q2601, V2.0", with minimum score of 80%

Assessor Requirements

Assessor Prerequisites						
Minimum Educational Qualification	**Specialization**	**Relevant Industry Experience**		**Training Experience**		**Remarks**
		Years	**Specialization**	**Years**	**Specialization**	
Graduate Science & Engineering	Electrical/ Mechanical/ Electronics	2	Semiconductor Technology, Embedded System	1	Semiconductor Technology, Embedded System	
Diploma/ITI	Electrical/ Mechanical/ Electronics	3	Semiconductor Technology, Embedded System	1	Semiconductor Technology, Embedded System	

Assessor Certification	
Domain Certification	**Platform Certification**
"**Foundation of System on Chip (SoC) Design**, ELE/MCr-0002, version 1.0". Minimum accepted score is 80%.	Recommended that the Assessor is certified forthe **Foundation of System on Chip (SoC) Design** "Assessor (VET and Skills)", mapped to the Qualification Pack: "MEP/Q2701, V2.0", with minimum score of 80%

Assessment Strategy

1. Assessment System Overview:
   - Batches assigned to the assessment agencies for conducting the assessment on SDMS/SIP or email
   - Assessment agencies send the assessment confirmation to VTP/TC looping SSC
   - Assessment agency deploys the ToA certified Assessor for executing the assessment
   - SSC monitors the assessment process & records

2. Testing Environment:
   - Confirm that the centre is available at the same address as mentioned on SDMS or SIP
   - Check the duration of the training.
   - Check the Assessment Start and End time to be as 10 a.m. and 5 p.m.
   - If the batch size is more than 30, then there should be 2 Assessors.
   - Check that the allotted time to the candidates to complete Theory & Practical Assessment is correct.
   - Check the mode of assessment—Online (TAB/Computer) or Offline (OMR/PP).
   - Confirm the number of TABs on the ground are correct to execute the Assessment smoothly.
   - Check the availability of the Lab Equipment for the particular Job Role.

3. Assessment Quality Assurance levels / Framework:
   - Question papers created by the Subject Matter Experts (SME)
   - Question papers created by the SME verified by the other subject Matter Experts
   - Questions are mapped with NOS and PC
   - Question papers are prepared considering that level 1 to 3 are for the unskilled & semi-skilled individuals, and level 4 and above are for the skilled, supervisor & higher management
   - Assessor must be ToA certified & trainer must be ToT Certified
   - Assessment agency must follow the assessment guidelines to conduct the assessment

4. Types of evidence or evidence-gathering protocol:

- Time-stamped & geotagged reporting of the assessor from assessment location
- Centre photographs with signboards and scheme specific branding
- Biometric or manual attendance sheet (stamped by TP) of the trainees during the training period
- Time-stamped & geotagged assessment (Theory + Viva + Practical) photographs & videos

5. Method of verification or validation:

   - Surprise visit to the assessment location
   - Random audit of the batch
   - Random audit of any candidate

6. Method for assessment documentation, archiving, and access

   - Hard copies of the documents are stored
   - Soft copies of the documents & photographs of the assessment are uploaded / accessed from Cloud Storage
   - Soft copies of the documents & photographs of the assessment are stored in the Hard Drives

References

Glossary

Term	Description
Key Learning Outcome	Key learning outcome is the statement of what a learner needs to know, understand and be able to do to achieve the terminal outcomes. A set of key learning outcomes will make up the training outcomes. Training outcome is specified in terms of knowledge, understanding (theory) and skills (practical/OJT application).
Training Outcome	Training outcome is a statement of what a learner will know, understand and be able to do **upon the completion of the training**
Terminal Outcome	Terminal outcome is a statement of what a learner will know, understand and be able to do **upon the completion of a module**. A set of terminal outcomes help to achieve the training outcome.
National Occupational Standard	National Occupational Standard specify the standard of performance an individual must achieve when carrying out a function in the workplace
Persons with Disability	Persons with Disability are those who have long-term physical, mental, intellectual, or sensory impairments which in interaction with various barriers may hinder their full and effective participation in society on an equal basis with others

Acronyms and Abbreviations

Term	Description
QF	Qualification File
NSQF	National Skills Qualification Framework
NSQC	National Skills Qualification Committee
NOS	National Occupational Standards
SSC	Skill Sectors Councils
NASSCOM	National Association of Software & Service Companies
NCO	National Classification of Occupations
ISO	International Organization for Standardization
SLA	Service Level Agreement
IT	Information Technology
CRM	Customer Relationship Management
PC	Performance Criteria
PwD	Persons with Disability
SOP	Standard Operating Procedure